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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,842	10/14/2003	Ken Gary Pomaranski	200310434-1	3525

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EXAMINER	
WU, JUNCHUN	
ART UNIT	**PAPER NUMBER**
2196	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/20/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/684,842	POMARANSKI ET AL.	
	Examiner	Art Unit	
	Junchun Wu	2196	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/14/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/07/2005;10/14/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detail Action

1. Claims 1-25 are pending in this application.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-5, 9-16, and 19-24 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-5, 8-12, and 14 of copending Application No. 1,069,0727, hereafter '727. Claims 1 and 15 of the instant application is directed to scheduling CPU cores for testing and scheduling execution of diagnostic code and program code on the selected execution units and remaining execution units respectively. These limitations are obvious from the limitations of claims 1 and 13 of '727. Dependent claims 2-5, 9-14, 16, and 19-24 of the instant application include similar limitations

as dependent claims 2-6, 8-12, and 14 of the '727. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 15-25 are rejected under 35 USC § 101 because the claimed invention is directed to non-statutory subject matter.

Claims 15 and 25 fail to claim the program recorded on an appropriate computer readable medium so as to be structurally and functionally interrelated to the medium and permit the function of the descriptive material to be realized. Claims 16-24, which depend from claim 15, are also rejected under 35 U.S.C. 101 for the same reasons.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 4-8, 15, 17-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Quach (US Patent No. 6,640,313 B1).

8. For claim 1, Quach teaches a method of compiling a program to be executed on a target microprocessor with multiple execution units of a same type (Fig.1 140(a)&(b) and col.4 lines 46-53), the method comprising: selecting one of the execution units for testing; scheduling execution of diagnostic code on selected execution unit; and scheduling execution of program code on remaining execution units of the same type (col.2 lines 32-41; instructions are provided by an issue module to processor's modes which are scheduling to run a diagnostic code in HR mode or scheduling to run program code in HP mode; running instructions on a processor in HR mode is interpreted as selecting such processor).

9. For claim 4, Quach teaches setting a level of aggressiveness for scheduling the testing of the execution units (col.2 lines 43-50; a check unit is activated in HR mode or deactivated in HP mode by compare executing result).

10. For claim 5, Quach teaches applying an aggressiveness-dependent algorithm to determine when to schedule all available units for execution of the program code and when to schedule parallel execution of the program code and the diagnostic code (col.10 lines 5-13; schedule instructions employed by various algorithm to run program code in HP mode or to run diagnostic code in HR mode).

11. For claim 6, Quach teaches a lowest level of aggressiveness comprises turning off said testing (col.2 lines 43-50; whenever a check unit is deactivated HR or HP mode the level of testing is off).

12. For claims 7 and 17, Quach teaches the multiple execution units of the same type comprise arithmetic logic units (Fig.1 includes IEU: integer execution unit; col.4 lines 46-50).

13. For claims 8 and 18, Quach teaches the multiple execution units of the same type comprise floating point units (Fig.1 includes FPU: floating point unit; col.4 lines 46-50).

14. For claim 15, Quach teaches:

A computer-readable program product for execution on a target microprocessor having multiple execution units of a same type integrated thereon (Fig.1 140(a)&(b) and col.4 lines 46-53), the program product comprising: diagnostic code configured to be executed on a selected execution unit of the multiple execution units; and program code configured to be executed on remaining execution units of the same type (col.2 lines 32-41; instructions are provided to processor's modes which are selected to run a diagnostic code in HR mode or selected to run program code in HP mode.)

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 9-14, 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quach, in view of Raina (US Patent No. 6,134,675).

17. For claims 9 and 19, Quach does not teach the multiple execution units comprise at least four execution units of the same type integrated onto the microprocessor integrated circuit, but Raina teaches the multiple execution units comprise at least four execution units of the same type integrated onto the microprocessor integrated circuit (Fig 1 & col.2 lines 7-10). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Quach's teachings by having the multiple execution units comprise at least four execution units of the same type integrated onto the microprocessor integrated circuit as taught by Raina in order to improve the method for testing multi-core processor integrated circuits (Raina col.1 lines 22-23).

18. For claims 10 and 20, Quach does not teach the scheduled diagnostic code performs diagnostic operations from a test pattern comprising operations with known expected results, but Raina teaches the scheduled diagnostic code performs diagnostic operations from a test pattern

comprising operations with known expected results (col.3 lines 19-22). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Quach's teachings the scheduled diagnostic code by performing diagnostic operations from a test pattern comprising operations with known expected results as taught by Raina in order to improve method that is better suited for testing integrated circuits containing multiple cores (Raina col.1 lines 22-23).

19. For claims 11 and 21, Raina discloses the scheduled diagnostic code compares an actual result with a known expected result (Raina col.3 lines 19-22).

20. For claims 12 and 22, Raina discloses the scheduled diagnostic code jumps to a fault handler if the compared results are different (col.3 lines 15-22).

21. For claims 13 and 23, Raina discloses the fault handler includes code to remove a faulty execution unit from use in executing code (col.3 lines 17-19).

22. For claims 14 and 24, Raina discloses the fault handler includes code to perform a system halt to prevent data corruption (col.3 lines 17-19).

23. Claims 2, 3, 16, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quach, in view of Murthi et al. (US Patent No. 5,673,388, hereafter Murthi).

24. For claim 2, Quach does not disclose the selection of the execution unit for testing utilizes an algorithm that assures testing of each of the multiple execution units, but Murthi teaches the selection of the execution unit for testing utilizes an algorithm that assures testing of each of the multiple execution units (col.7 lines 44-53 & Fig. 2; col.9 lines 56-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Quach teachings by utilizing an algorithm that assures testing of each of the multiple execution units as taught by Murthi in order to provide a faster way of initializing a multiple processor computer system and increase the speed of testing in the multiple processor system (Murthi col.2 lines 11-13).

25. For claim 3, Quach and Murthi do not disclose the algorithm comprises a round-robin type algorithm. Official notice is taken that the use of round-robin type algorithm is a well-known and expected in the art. It would have been obvious to one skilled in the art at the time of the invention to implement in Quach and Murthi a round-robin algorithm in order to scheduling task for processes in an operating system, which assigns time slices to each process in equal portions and in order. Round-robin algorithm may be used to effectively schedule the task on the CPU where each process is given equal time in a cycling list.

26. For claim 16, Quach does not teach the selected execution unit rotates between the multiple execution units such that each execution unit is tested, but Murthi teaches the selected execution unit rotates between the multiple execution units such that each execution unit is tested (col.7 lines 44-53 & Fig. 2; in a multiprocessor system, bootstrap processor (BSP) oversee the initialization and perform the bulk of initialization tests for each processor other than BSP). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Quach's teachings by the selected execution unit rotates between the multiple execution units such that each execution unit is tested as taught by Murthi in order to provide a faster way of initializing a multiple processor computer system and increase the speed of testing in the multiple processor system (Murthi col.2 lines 11-13).

27. For claim 25, Quach teaches a computer-readable program product for execution on a target microprocessor having multiple execution units of a same type integrated thereon (Fig.1 140(a)&(b) and col.4 lines 46-53), the program product comprising: diagnostic code configured to be executed on a selected execution unit of the multiple execution units (col.2 lines 32-41; instructions are provided to processor's modes which are selected to run a diagnostic code in HR mode or selected to run program code in HP mode.), and wherein said diagnostic code is further configured to be run in a background type process on a multi-threaded operating system (col.3 lines 32-35; diagnostic code can associate the operating system kernel code executing in the HR mode). Quach does not teach the selected execution unit rotates between the multiple execution units such that each execution unit is tested. However, Murthi teaches the selected execution unit rotates between the multiple execution units such that each execution unit is tested (col.7

lines 44-53 & Fig. 2; in a multiprocessor system, bootstrap processor (BSP) oversee the initialization and perform the bulk of initialization tests for each processor other than BSP). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Quach's teachings by the selected execution unit rotates between the multiple execution units such that each execution unit is tested as taught by Murthi in order to provide a faster way of initializing a multiple processor computer system and increase the speed of testing in the multiple processor system (Murthi col.2 lines 11-13).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junchun Wu whose telephone number is 571-270-1250. The examiner can normally be reached on Flexible.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nabil El-hady can be reached on 571-272-3963. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Junchun Wu